02935.000001. PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
	:	Examiner: NYA
LUC BURGUN ET AL.	)	
	:	Group Art Unit: NYA
Application No.: NYA	)	
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Filed: Herewith	)	
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For: METHOD AND SYSTEM FOR EMULATING A DESIGN UNDER TEST ASSOCIATED WITH A TEST ENVIRONMENT	)	
	:	June 25, 2003

Mail Stop New Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PRELIMINARY AMENDMENT

Sir:

Preliminary to examination, please amend the above-identified application, filed herewith, as follows:

IN THE CLAIMS

Please amend the Claims 5, 6, 8, 13-17, 19, 20, and 25 as follows:

1. (Original) Method of emulating a design under test associated with a test environment, characterized in that it comprises two distinct generating phases

comprising a first phase of generating (80) a first file (FCH1) for configuring the test environment, and a second phase of generating (81) a second file (FCH2) for configuring at least a part of the design under test, the delivery of the first configuration file to a first reconfigurable hardware part (BTR) forming a reconfigurable test bench so as to configure the test bench, and the delivery of the second configuration file to a second reconfigurable hardware part (EML) so as to configure an emulator of the design under test, the two hardware parts being distinct and mutually connected.

2. (Original) Method according to claim 1, characterized in that the first generating phase (80) comprises the production (800) of a logic circuit (CRL) consisting of a network of logic gates and representative of the test environment as well as of the compilation directives, and a compilation (801) of this logic circuit having regard to the said directives, so as to obtain the first configuration file (FCH1).

3. (Original) Method according to claim 2, characterized in that the test environment comprises a collection of drivers (PLi) and of monitors (MNi), and in that the production of the said logic circuit comprises the formation of hardware blocks in the form of networks of logic gates, these hardware blocks representing interfaces of drivers/monitors of software stimulation, interfaces of drivers/monitors of real hardware stimulation, and drivers/monitors of emulated hardware stimulation, blocks for calculations

of hardware triggers, as well as a block for interfacing with the emulator of the design under test.

4. (Original) Method according to claim 3, characterized in that the phase of forming the hardware blocks is effected on the basis of statically defined networks of gates or of networks of gates which are generated dynamically by a software module.

5. (Currently Amended) Method according to any one of ~~the preceding~~ claims 1 to 4, characterized in that the first generating phase (80) and the second generating phase (81) are performed in parallel.

6. (Currently Amended) Method according to any one of claims 1 to 4, characterized in that the first generating phase (80) and the second generating phase (81) are performed sequentially.

7. (Original) Method according to claim 6, characterized in that the first generating phase (80) is performed before or after the second generating phase (81).

8. (Currently Amended) Method according to ~~claims~~ claim 3 ~~and 7~~, characterized in that when the first generating phase is performed after the second generating phase, the production of the logic circuit (CRL) uses as input parameters a

description of the assignment of the logic inputs/outputs of the design under test to the pins of the emulator, and in that when the second generating phase is performed after the first generating phase, the production of the logic circuit uses as input parameters a description of the interface of the design under test and supplies as output a description of the assignment of the logic inputs/outputs of the design under test to the pins of the emulator, this output description then being a constraint parameter for the second generating phase.

9. (Original) Emulation system, intended to emulate a design under test associated with a test environment, characterized in that it comprises a reconfigurable hardware test bench (BTR) capable of emulating a part at least of the test environment, this test bench being connected between a host computer and a reconfigurable hardware emulator (EML), distinct from the test bench, and capable of emulating at least a part of the design under test, first generating means able to generate a first file for configuring the test environment, and second generating means able to generate a second file for configuring the design under test.

10. (Original) System according to claim 9, characterized in that the reconfigurable test bench (BTR) comprises a so-called fixed part and at least one reconfigurable interface circuit (CRFG) capable of embodying the emulated part of the test environment.

11. (Original) System according to claim 10, characterized in that the fixed part comprises at least one control circuit (CCTL) and one circuit (CIBS) for interfacing with the host computer, and in that the reconfigurable interface circuit is able to comprise at least interfaces of drivers/monitors of software stimulation which are capable of establishing a communication with at least one software process executed on the host computer, and drivers/monitors of emulated hardware stimulation.

12. (Original) System according to claim 11, characterized in that the fixed part furthermore comprises additional real hardware drivers/monitors, and in that the reconfigurable circuit (CRFG) is able furthermore to comprise interfaces with these additional real hardware drivers/monitors.

13. (Currently Amended) System according to any one of claims 9 to 12, characterized in that the fixed part furthermore comprises a circuit (IFSC) for interfacing with a target device (SYC).

14. (Currently Amended) System according to ~~one of claims~~ claim 9 ~~to 13~~, characterized in that the fixed part furthermore comprises the control part of a hardware logic analyser (AL) whose state evolves as a function of the hardware triggers.

15. (Currently Amended) System according to ~~one of claims~~ claim 9 ~~to~~ ~~14~~, characterized in that the reconfigurable test bench comprises a clock signals generator synchronized by a base system clock and delivering various secondary clock signals synchronizing the emulator of the design under test and certain at least of the hardware means of the test bench, as well as clock retrocontrol means capable in response to at least one wait signal transmitted by one of the hardware means of the test bench regulated by a first secondary clock signal of temporarily disabling certain of the other secondary clock signals with different frequencies from that of the first secondary clock signal.

16. (Currently Amended) System according to ~~one of claims~~ claim 9 ~~to~~ ~~15~~, characterized in that the test bench and the emulator are embodied on an electronic card external to the host computer and connected to the latter's mother card.

17. (Currently Amended) System according to ~~one of claims~~ claim 9 to ~~15~~, characterized in that the reconfigurable test bench is embodied on a first electronic card external to the host computer and connected to the latter's mother card, and in that the emulator of the design under test is embodied on one or more other cards external to the host computer and connected to the said first external card.

18. (Original) System according to claim 17, characterized in that the circuit for interfacing with the target device is integrated into the said first external card.

19. (Currently Amended) System according to any one of claims 10 to ~~16~~ 12, characterized in that the test bench and the emulator are embodied on an internal electronic card (CINT) incorporated into the host computer.

20. (Currently Amended) System according to ~~claims~~ claim 13 ~~and 19~~, characterized in that the circuit for interfacing with the target device is embodied on an external electronic card (CXT) outside the host computer, and able to be connected to the said internal electronic card (CINT).

21. (Original) Electronic card, intended to be connected to the mother card of a host computer, characterized in that it comprises a reconfigurable hardware test bench (BTR) capable of emulating a part at least of a test environment associated with a design under test, and a reconfigurable hardware emulator (EML), distinct from the test bench, connected to the reconfigurable test bench and capable of emulating at least a part of the design under test.

22. (Original) Card according to claim 21, characterized in that the reconfigurable test bench (BTR) comprises a so-called fixed part and at least one reconfigurable circuit capable of embodying the emulated part of the test environment.

23. (Original) Card according to claim 22, characterized in that the fixed part comprises at least one control circuit (CCTL) and one circuit for interfacing with the host computer, and in that the reconfigurable circuit is able to comprise at least interfaces of drivers/monitors of software stimulation which are capable of establishing a communication with at least one software process executed on the host computer, and drivers/monitors of emulated hardware stimulation.

24. (Original) Card according to claim 23, characterized in that the fixed part furthermore comprises additional real hardware drivers/monitors, and in that the reconfigurable circuit is able to comprise further interfaces with these additional real hardware drivers/monitors.

25. (Currently Amended) Card according to any one of claims 21 to 24, characterized in that the reconfigurable test bench comprises a clock signals generator synchronized by a base system clock and delivering various secondary clock signals of different frequencies, as well as clock retrocontrol means capable in response to a wait signal transmitted by one of the hardware means of the test bench regulated by a first secondary clock signal of temporarily disabling the secondary clock signals with different frequencies from that of the first secondary clock signal.